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Paper No. 24

Application Number: 09/020,647
Filing Date: February 09, 1998
Appellant(s): FJELSTAD ET AL.

Michael J. Doherty
For Appellant

EXAMINER'S ANSWER

This is in response to appellant's brief on appeal filed 5-21-01.

(1) Real Party in Interest

A statement identifying the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

A statement identifying the related appeals and interferences which will directly affect or be directly affected by or have a bearing on the decision in the pending appeal is contained in the brief.

(3) Status of Claims

The statement of the status of the claims contained in the brief is correct.

(4) Status of Amendments After Final

Appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Invention

The summary of invention contained in the brief is correct.

(6) Issues

Appellant's statement of the issues in the brief is substantially correct. The changes are as follows:

Whether claims 1-4, 6-7, 11, 21-23, 25-30 and 33-34 are unpatentable under 35 U.S.C. § 102(b) as anticipated by U.S. Patent 5,070,297 to *Kwon et al.* ("*Kwon*").

(7) Grouping of Claims

Appellant's brief includes a statement that claims 1-11, 21-23 and 25-34 do not stand or fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

(8) Claims Appealed

The copy of the appealed claims contained in the Appendix to the brief is correct.

(9) Prior Art of Record

5,070,297	KWON et al.	12-1991
5,874,782	PALAGONIA	2-1999

(10) Grounds of Rejection

In the rejections infra, reference labels are generally recited only for the first recitation of identical claim language.

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34 stand rejected under 35 U.S.C. 102(b) as anticipated by Kwon (5070297).

At column 4, line 13 to column 7, line 34, Kwon teaches the following:

1. A method of creating a compliant semiconductor chip package assembly comprising the steps of providing a first dielectric

protective layer 34 on a contact bearing surface of a semiconductor chip 14, wherein the semiconductor chip has a central region bounded by chip contacts 36 of the semiconductor chip and wherein the dielectric protective layer has a plurality of apertures such that the chip contacts are exposed; providing a compliant layer 32 atop the first dielectric protective layer within the central region, wherein said compliant layer has a substantially flat top surface, a bottom surface that is attached to the first dielectric protective layer and sloping edges between the top surface and the bottom surface; and selectively electroplating elongated bond ribbons 28 atop the first dielectric protective layer and the compliant layer wherein each bond ribbon electrically connects each chip contact to a respective conductive terminal 20-22-24 on the top surface of the compliant layer, and wherein said elongated bond ribbons extend along the sloping edges of said compliant layer.

2. The method according to Claim 1 further including the step of providing a second dielectric protective layer 26 atop exposed assembly elements 28 on the terminal side of the assembly after the step of selectively electroplating the bond ribbons, wherein the second dielectric protective layer has a plurality of apertures such that the terminals are exposed.

3. The method according to Claim 1 wherein the compliant layer material is selected from the group consisting of silicone, flexibilized epoxy, a thermosetting polymer, fluoropolymer, thermoplastic polymer, polyimide, foams and combinations or composites thereof.

4. The method according to Claim 1 further including the step of providing for an encapsulant layer 26 atop an exposed surface of the bond ribbons.

6. The method according to Claim 4 further including the step of providing for a second dielectric protective layer 21 atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures such that terminal positions are exposed.

7. The method according to Claim 1 wherein a silicon dioxide passivation layer on the face surface of the semiconductor chip comprises the first dielectric protective layer.

11. The method according to Claim 1 wherein the sloping edges of the compliant layer have a first transition region near the top surface of the compliant layer and a second transition region near the bottom surface of the compliant layer and wherein both the first transition region and the second transition region have a radius of curvature.

21. A method of making a compliant microelectronic assembly comprising the steps of: providing a microelectronic element 38 having a first surface and a plurality of contacts 36 disposed on the first surface thereof; providing a compliant layer 32 over the first surface of said microelectronic element, said compliant layer having a bottom surface facing toward said first surface of said microelectronic element, a top surface facing upwardly away from said microelectronic element and one or more edge surfaces extending between said top and bottom surfaces, and then selectively forming elongated, flexible bond ribbons 28 over said compliant layer so that said bond ribbons extend over said top surface and one or more of said edge surfaces and said bond ribbons electrically connect said contacts to conductive terminals 20-22-24 overlying the top surface of said compliant layer.

22. The method as claimed in claim 21, wherein said contacts on said microelectronic element are disposed in a first region of said first surface, said compliant layer overlies a second region of said first surface, and one or more edge surfaces include one or more border edge surfaces extending along one or more borders between said first and second regions.

23. The method as claimed in claim 21, wherein said selectively forming bond ribbons step includes selectively electroplating said bond ribbons.

25. The method as claimed in claim 21, further comprising the step of: before the providing a compliant layer step, providing a first dielectric protective layer 34 on the first surface of the microelectronic element, the first dielectric layer having a plurality of apertures therein so that said contacts are accessible therethrough, the providing the compliant layer step including the step of providing the compliant layer over said first dielectric protective layer.

26. The method as claimed in claim 25, the selectively forming flexible bond ribbons step including selectively electroplating said bond ribbons atop said first dielectric protective layer and said compliant layer.

27. The method as claimed in claim 21, further including the step of providing a dielectric cover layer 21 over said compliant layer and said bond ribbons after the step of selectively forming the bond ribbons, wherein the cover layer has a plurality of apertures so that said terminals are accessible therethrough.

28. The method as claimed in claim 21, further including the step of providing an encapsulant layer 26 over an exposed surface of the bond ribbons.

29. The method as claimed in claim 28, further including the step of providing a second dielectric protective layer 21 atop the encapsulant layer wherein the second dielectric protective layer has a plurality of apertures so that said terminals are accessible therethrough.

30. The method as claimed in claim 21, further including the step of depositing a barrier metal 30 atop said contacts, prior to the step of forming the bond ribbons, whereby the barrier metal (inherently) helps to prevent voiding between the contacts and the bond ribbons.

33. The method as claimed in claim 21, wherein the edge surfaces of the compliant layer are sloping surfaces which extend in both vertical and horizontal directions.

34. The method as claimed in claim 33, wherein at least some of said sloping edge surfaces have first transition regions near the top surface of the compliant layer and second transition regions near the bottom surface of the compliant layer, and wherein both the first and second transition regions have respective radii of curvature.

To further clarify the teaching of forming elongated bond ribbons 28, it is noted that Kwon teaches at, for example, Figure 2, that the contacts 28 are small and narrow in width in proportion to length or height; therefore, the contacts are elongated.

To further clarify the teaching of first transition regions near the top surface of the compliant layer and second transition regions near the bottom surface of the compliant layer, it is noted that it is inherent that the first and second regions near the top and bottom surface, respectively, transition into neighboring regions of the compliant layer and other neighboring layers.

To further clarify the teaching wherein both the first and second transition regions have respective radii of curvature, it is noted that it is inherent in the process of Kwon that the regions have radii equal to zero or greater because the radii are line segments and line segments have radii of curvature equal to zero or greater.

Claims 5 and 8 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon (5070297).

Kwon is applied as it was applied to claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34.

As cited supra, Kwon teaches the following:

8. The method according to Claim 1 further including the step of plating a barrier metal 30 atop the semiconductor chip contacts, whereby the barrier metal (inherently) helps to prevent voiding at the boundary between the semiconductor chip contacts and the bond ribbons. However, Kwon does not appear to explicitly teach the practice of this step prior to the step of providing the compliant layer. Nonetheless, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed sequence because appellant has not disclosed that the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical. In fact, there is no support for this claim limitation elsewhere in the disclosure. Moreover, it is well established that, in a well known process, the order of performing process steps is prima facie obvious in the absence of new or unexpected results. *Ex parte Rubin 128 USPQ (PO BdPatApp 1959)*.

Kwon also does not appear to explicitly teach the following:

5. The method according to Claim 4 wherein the encapsulant layer material is selected from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel. Nonetheless, as

cited, Kwon teaches that "Protective coating 26 may comprise any number of compliant materials having sufficient elastic, protective, and adhesive properties for the purposes of the present invention." Furthermore, judicial notice is taken that it is well known to select protective coating encapsulant layers from the group consisting of silicone, flexibilized epoxy, thermoplastic and gel. Moreover, it would have been obvious to combine the well known process with the process of Kwon because it would provide a protective coating. It is noted that appellant has not seasonably traversed this well known statement. Thus, as set forth in MPEP 2144.03:

> If applicant does not seasonably traverse the well known statement during examination, then the object of the well known statement is taken to be admitted prior art. In re Chevenard, 139 F.2d 71, 60 USPQ 239 (CCPA 1943). A seasonable challenge constitutes a demand for evidence made as soon as practicable during prosecution. Thus, applicant is charged with rebutting the well known statement in the next reply after the Office action in which the well known statement was made.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 9, 10, 31 and 32 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon as applied to

claims 1-4, 6, 7, 11, 21-23, 25-30, 33 and 34 supra, and further in combination with Palagonia (5874782).

As cited supra, Kwon teaches the following:

9. The method according to Claim 1 applied simultaneously to a multiplicity of undiced semiconductor chips 14 on a wafer 10 to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

10. The method according to Claim 1 applied simultaneously to a multiplicity of adjacent semiconductor chips 14 arranged in an array to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

31. The method as claimed in claim 21, the method being applied to a plurality of undiced semiconductor chips 14 on a wafer 10 to form a corresponding plurality 12 of compliant semiconductor chip packages 14.

32. The method as claimed in claim 21, the method being applied to a plurality of adjacent semiconductor chips 14 arranged in an array to form a corresponding multiplicity 12 of compliant semiconductor chip packages 14.

However, Kwon does not appear to explicitly teach:

9. The method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

10. The method further including the step of dicing the packages following the step for selectively electroplating the bond ribbons.

31. The method further including the step of separating the packages following the step of depositing the bond ribbons.

32. The method further including the step of separating the packages following the step of selectively electroplating the bond ribbons.

Nevertheless, at column 3, line 1 to column 6, line 19, Palagonia teaches a method including a step of dicing and separating a plurality of adjacent compliant semiconductor chip packages 22 arranged in an array on a wafer 20 following a step of selectively electroplating bond ribbons 26. Moreover, it would have been obvious to combine the process of Palagonia with the process of Kwon because it would facilitate testing of individual chips.

(11) Response to Argument

Appellant contends that Kwon does not teach "wherein elongated bond ribbons extend along the sloping edges of said compliant layer." This contention is respectfully traversed because as cited, particularly at column 5, lines 15-18, Kwon teaches that the ribbons 28 are "V-shaped," and further illustrates in Figure 2 that the V-shaped ribbons are small and

narrow in width in proportion to length or height (hence elongated) along the sloping edges of compliant layer 32.

Also, appellant alleges that Kwon does not teach that the bond ribbons are curved. This allegation is respectfully deemed to be unpersuasive because the scope of the claims is not so limited, and Kwon is not applied to the rejection for this teaching. To further clarify, claim 11 is limited to a process wherein the first and second transition regions of the compliant layer, and not the bond ribbons, have a radius of curvature. Moreover, the limitation that the compliant layer transition regions have a radius of curvature does not limit the transition regions to regions that are curved. For example, a straight line has a radius of curvature of infinity, and of course, a straight line is not curved.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully Submitted,

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Conferees:

Arthur Grimley AM

Olik Chaudhuri OC.

DEG
July 25, 2001